IN THE CLAIMS

What is claimed is:

1. A flat panel display, comprising:

a substrate;

a pixel electrode having an opening portion formed on said substrate;

a semiconductor layer formed over a surface of said substrate that is spaced apart from said pixel electrode and having source and drain regions formed at both end portions thereof;

a first insulating layer formed over the surface of said substrate except over the opening portion of said pixel electrode;

a gate electrode formed on said first insulating layer over said semiconductor layer; and

a second insulating layer formed over the surface of said substrate except the opening portion of said pixel electrode.

2. The flat panel display of claim 1, further comprising:

contact holes formed in said first and second insulating layers, which expose a portion of said pixel electrode and portions of the source and drain regions of said semiconductor layer;

source and drain electrodes formed on said second insulating layer, wherein the source electrode is electrically connected to the source region through one of the contact holes, and the drain electrode is electrically connected to the drain region and said pixel electrode through another one of the contact holes; and

a third insulating layer formed over the surface of said substrate except the opening portion of said pixel electrode.

3. The flat panel display of claim 2, wherein the third insulating layer is a planarization layer comprising one of an oxide layer, a nitride layer, SiNx, SiOx, and acryl.

4. The flat panel display of claim 3, wherein the opening portion has an area sized to be smaller than an area of said pixel electrode.

5. The flat panel display of claim 2, wherein the third insulating layer is a planarization layer that is made of a photoresist layer.

6. The flat panel display of claim 1, wherein the opening portion has an area sized smaller than an area of said pixel electrode.

7. A method of manufacturing a flat panel display, comprising:

forming a pixel electrode and a semiconductor layer, spaced apart from each other, on a substrate;

forming a first insulating layer over a surface of the substrate to cover the pixel electrode and the semiconductor layer;

forming a gate electrode on a portion of the first insulating layer corresponding to a location of the semiconductor layer;

forming a second insulating layer over the surface of the substrate to cover the gate electrode;

forming contact holes in the first and second insulating layers to expose a portion of the pixel electrode and portions of the semiconductor layer;

forming source and drain electrodes on the second insulating layer electrically connecting the source electrode to the semiconductor layer through one of the contact holes, and electrically connecting the drain electrodes to the semiconductor layer and the pixel electrode through another one of the contact holes;

forming a photoresist layer over the surface of the substrate exposing a portion of the second insulating layer over the pixel electrode; and

forming an opening portion by etching the first and second insulating layers using the photoresist layer as a mask.

8. The method of claim 7, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode after forming the semiconductor layer.

9. The method of claim 7, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode before forming the semiconductor layer.

10. The method of claim 7, wherein said forming of the semiconductor layer comprises:

forming a polysilicon layer on the substrate; and

patterning the polysilicon layer to form the semiconductor layer.

11. The method of claim 7, wherein said forming of the semiconductor layer comprises:

depositing an amorphous silicon layer on the substrate;

annealing the amorphous silicon layer to form a polysilicon layer; and

patterning the polysilicon layer to form the semiconductor layer.

12. The method of claim 7, wherein said forming of the semiconductor layer comprises:

forming a polysilicon layer on the substrate; and

patterning the polysilicon layer to form the semiconductor layer.

13. The method of claim 12, wherein said forming of the gate electrode comprises:

depositing a first metal layer on the first insulating layer; and

patterning the first metal layer to form the gate electrode.

14. The method of claim 13, further comprising forming source and drain regions at corresponding end portions of the semiconductor layer.

15. The method of claim 14, wherein said forming of the source and drain electrodes comprises:

depositing a second metal layer on the second insulating layer; and

patterning the second metal layer to form the source and drain electrodes.

16. The method of claim 15, wherein said forming of the opening portion comprises using the remaining photoresist layer as a planarization layer.

17. The method of claim 16, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode after forming the semiconductor layer.

18. The method of claim 16, wherein said forming of the pixel electrode and the semiconductor layer comprises forming the pixel electrode before forming the semiconductor layer.

19. The method of claim 15, further comprising:

forming a third insulating layer over the surface of the substrate before the forming of the photoresist layer; and

removing the remaining photoresist layer after the forming of the opening portion using the photoresist layer as a mask.

20. The method of claim 19, wherein the third insulating layer comprises one of an oxide layer, a nitride layer and an acryl layer.

21. The method of claim 7, wherein said forming of the opening portion comprises using the remaining photoresist layer as a planarization layer.

22. The method of claim 7, further comprising:

forming a third insulating layer over the surface of the substrate before the forming of the photoresist layer; and

removing the remaining photoresist layer after the forming of the opening portion using the photoresist layer as a mask.